APPLICATION UNDER UNITED STATES PATENT LAWS

Invention: **MODERATE CURRENT 5V TOLERANT BUFFER USING A 2.5 VOLT POWER SUPPLY**

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This is a:

[ ] Provisional Application

[X] Regular Utility Application

[ ] Continuing Application

[ ] PCT National Phase Application

[ ] Design Application

[ ] Reissue Application

[ ] Plant Application

SPECIFICATION

MODERATE CURRENT 5V TOLERANT BUFFER USING A 2.5 VOLT POWER SUPPLY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to buffers. More particularly, it relates to integrated circuits (ICs) including low voltage buffers, e.g., 2.5 volt buffers having high current and/or voltage tolerance.

2. Background of Related Art

In computer systems, the reduction of power usage is paramount. Initially, many computer buses (e.g., SCSI, DDR, PCI, PCMCIA, etc.) were based on 5 volt standards. More recently, the voltage level of those standards has been lowered to 3.3 volts. The lower voltage provides significant power savings, lowers capacitance between lines, and other advantages.

However, in lowering the voltage standard to 3.3V, many existing system components would have been rendered useless but for requirements that the new, lower voltage systems be backwards compatible to accommodate 5V components. Thus, system components generally powered at only 3.3V needed to communicate with system components that were powered at 5V. The terminology referring to this backwards compatibility for 5V legacy systems is commonly referred to as "5V tolerant" systems.

Various system components communicate with one another typically via wired lines or busses. To buffer various components, input and/or output buffers are typically established at the input or output of any line in communication with the bus or lines to another system component. Many systems have bi-directional communication lines, and bi-directional buffers are appropriately used.

5V tolerant, 3.3V buffers have been known. For instance, Fig. 7 shows a portion of an integrated circuit including conventional 5V tolerant open drain buffer made with 3.3V technology MOS transistors.

In particular, as shown in Fig. 7, **VDD** represents the power supply, and **VSS** ground. An inverter formed by a series connection of a p-channel Field Effect Transistor (FET) **M1** and an n-channel FET transistor **M2** drives node **N** to the opposite voltage of the input signal **A**. An output stage comprises a series connection of two n-channel FET transistors **M3** and **M4**. The gate of transistor **M3** is connected to node **N**, while the gate of transistor **M4** is connected to the power supply **VDD**.

In operation, when signal **A** is LOW, node **N** goes HIGH, turning transistor **M3** ON and pulling **PAD** LOW, since transistor **M4** is always ON. When signal **A** is HIGH, node **N** is driven LOW, turning transistor **M3** OFF.

If a 5V signal is applied to **PAD** when signal **A** is HIGH, transistor **M4** protects transistor **M3** by acting as a source-follower. Thus, when **PAD** is at 5V, transistor **M4** does not allow node **N1** to go below **VDD**-Vtn, where Vtn is the n-channel threshold of transistor **M4**. This value is typically 0.8V. With a nominally 3.3V +/- 10% power supply (**VDD**=3.3V), the voltage at node **N1** cannot go below 3.0V - 0.8V = 2.2V. On the other hand, with a maximum voltage of 5V + 10% = 5.5V on **PAD** (high end range of a nominally 5.0V power supply), this limits the drain-to-source voltage on transistor **M4** to 5.5V - 2.2V = 3.3V.

In the never-ending quest to lower power consumption and increase the speed of electronic and computer systems, lower voltage standards are being developed, most notably a 2.5V standard. Over the years this standard may drop to 2.0V, and even to 1.8V. For such low voltage systems to maintain support for and compatibility with legacy systems, it is desirable for 2.5V systems to be capable of communicating and fully operable with systems using nominal 5V and 3.3V power

supplies. However, significant hurdles exist for such ultra low voltage 2.5V (and less) systems to be tolerant to 5V inputs or outputs.

For instance, while power supplies have a nominal voltage of, e.g., 5V or 2.5V, etc., power supplies typically exhibit a tolerance in voltage variation of +/- 10%. Tight tolerances on a power supply dramatically increases costs of the power supply. As in everything, there is a balance between acceptable tolerance and price. Many power supplies are considered acceptable with a +/- 10% tolerance. Thus, even though a power supply might be nominally rated for 2.5V, it can be as low as 2.25V. Similarly, even though a 5.0V system is nominally rated for 5.0V, it can be as high as 5.5V.

Referring again to the conventional buffer **500** shown in Fig. 7, if **VDD** were to be lowered to only 2.25V, then node **N1** can go as low as 2.25V - 0.8V = 1.45V. This generates a drain-to-source voltage on transistor **M4** equal to 5.5V - 1.45V = 4.05V. This voltage of over 4 volts significantly exceeds the high end technology limit of 3.63V for 3.3V technology. Thus, the transistors of the buffer **500** would be damaged if **VDD** were an in-spec 2.25V and an in-spec 5.5V legacy system were connected to the buffer **500**.

Current 5V tolerant buffers manufactured using 3.3V technology require a 3.3V power supply to assure that no transistor sees a gate voltage or drain-to-source voltage greater than 3.63V. There is a need for an integrated circuit having a 5V tolerant buffer design that can be powered with a power supply voltage significantly lower than 3.3 V, e.g., of only a 2.5V (or lower voltage).

BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of the present invention will become apparent to those skilled in the art from the following description with reference to the drawings, in which:

Figs. 1 and 2 show a portion of an integrated circuit including a high current, 5V tolerant 2.5V (or lower voltage) open drain output buffer, in accordance with a first embodiment of the present invention.

Fig. 3 shows the embodiment of Figs. 1 and 2 implemented as an open drain bi-directional buffer.

Fig. 4 shows a backgate bias generator formed on an integrated circuit, and Fig. 5 shows an example of a more moderate current, 5V tolerant 2.5V (or lower voltage) open drain output buffer utilizing the backgate bias generator, in accordance with another embodiment of the present invention.

Fig. 6 shows an integrated circuit including the embodiment of Figs. 4 and 5 implemented as an open drain bi-directional buffer.

Fig. 7 shows an integrated circuit including a conventional 5V tolerant open drain buffer made with 3.3V technology MOS transistors.

SUMMARY OF THE INVENTION

In accordance with the principles of the present invention, a low voltage, 5V tolerant buffer comprises an inverter, and a current path-series connection of at least three transistors. An end of an upper transistor in the current path-series connection is connected to a PAD, and an end of a lower transistor of the series connection is connected to ground. A bias generator has an output connected to a gate of the upper transistor. A gate of a central one of the current path series connection of three transistors is connected to a power supply of no greater than 2.5V nominal. Typically the buffer is manufactured as part of an IC, though it could alternatively be manufactured as separate components.

In accordance with another aspect of the invention, a method of providing a low voltage, 5V tolerant buffer comprises adapting an input signal for inversion. A current path-series connection of at least three transistors is provided. A terminal of an upper transistor in the current path-series connection is connected to a PAD. A terminal of a

lower transistor of the current path-series connection is connected to ground. A bias voltage is provided to a gate of the upper transistor. The bias voltage is based on a difference between a power supply voltage and a voltage at the PAD. A power supply input is coupled to a gate of a central one of the current path-series connection of three transistors.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The embodiments of the present invention are designed for use with a power supply of a 2.5V nominal power supply. Nominal as used herein relates to the acknowledgement that actual power varies within a reasonable tolerance, e.g., most often +/10%. Thus, a nominal 2.5V power supply may actually produce anywhere between 2.25V and 2.75V. The disclosed embodiments are equally applicable for operation with voltage supplies as low as 2.0V nominal, and possibly as low as 1.8V nominal.

Some buffers are required to tolerate an input voltage greater than that allowed by the particular semiconductor technology. For instance, circuits that allow a 3.3V technology to tolerate a 5V signal applied to the buffer's pad have long been known. However, such circuits require a power supply of 3.3V to tolerate the 5V signal. The circuitry and methods described herein provide similar high voltage/current tolerance to be achieved with only a 2.5V power supply.

In a first embodiment, the buffer is determined to be area efficient for sink currents greater than about 30-40mA. In a second embodiment, the buffer is determined to be area efficient for sink currents less than about 24 mA.

In all disclosed embodiments, the buffer (input, output, or bidirectional buffer) is an open drain buffer. It will be understood by those of ordinary skill in the art that the circuit described herein to provide an improved open drain buffer can also be used in the pull-down portion of a push-pull buffer.

Figs. 1 and 2 show a portion of an integrated circuit including a 5V tolerant 2.5V (or lower voltage) open drain output buffer, in accordance with a first embodiment of the present invention.

In particular, as shown in Fig. 1, a comparator **102** is used to generate an indicator signal **NORM** as to whether the signal on a particular signal line input is at the same voltage level as the buffer, or is higher (e.g., 5V) and thus requiring legacy backwards compatibility in the buffer. The comparator **102** has the power supply **VDD** of the buffer input into its non-inverting input (+), and a voltage level of the relevant input at the inverting input (-). The comparator **102** evaluates the difference in voltages between the power supply voltage **VDD**, and the voltage level of the relevant **PAD**. If **VDD** is greater than or essentially equal to **PAD**, then the legacy present signal **NORM** is driven HIGH by the comparator **102**. On the other hand, if **VDD** is less than **PAD**, as is the case when 5V is applied to the **PAD**, then the legacy present signal **NORM** is driven LOW. It will be appreciated by those of ordinary skill in the art that the opposite signal levels may alternatively be implemented, i.e., with the legacy present signal **NORM** being driven HIGH if **PAD** is greater than **VDD**.

Appropriate hysteresis may be implemented in the comparator **102** to avoid oscillation when the **PAD** voltage is essentially the same as **VDD**.

Fig. 2 shows how the legacy present signal **NORM** may be utilized to instigate 5V tolerance in the output buffer **100**, which uses a nominal power supply of **VDD**=2.5V in the disclosed embodiments.

In particular, as shown in Fig. 2, a p-channel FET transistor **M5** has its current path connected between a power supply voltage **VDD** and a node **N1**. The node **N1** is connected to a node between two series coupled output FET transistors **M3** and **M4**. The current path of transistor **M4** is connected between the **PAD** and node **N1**, and the current path of transistor **M3** is connected between the node **N1** and **VSS**, which is typically at ground potential.

The gate of the second transistor **M3** is driven from a node **N**, formed between the series current path of a p-channel FET transistor **M1** and an n-channel FET transistor **M2**. The other side of the current path of transistor **M1** is connected **VDD**, which is typically at power supply potential, and the other side of the current path of transistor **M2** is connected to **VSS**. The gates of the transistors **M1**, **M2** are tied together forming node **A**, and are driven by a signal applied thereto.

In operation, when a 5V signal is applied to **PAD**, indicating that a legacy device is present and connected to the buffer **100**, the legacy present signal **NORM** is driven low, turning transistor **M5** ON. This connects node **N1** to the power supply **VDD** electrically, and ensures that the minimum voltage at node **N1** is **VDD**. Thus, the drain-to-source voltage on transistor **M4** becomes limited to a maximum value of 5.5V - 2.25V = 3.25V. On the other hand, when **PAD** is less than (or essentially equal to) the 2.5V power supply **VDD**, the legacy present signal **NORM** is driven HIGH, turning transistor **M5** OFF.

However, transistors **M3** and **M4**, no matter how large, are not sufficient to protect the buffer **100**, particularly from the damaging effects of an electro-static discharge (ESD) event. Transistors provided for ESD protection are large transistors, which are typically made from many smaller transistors connected in parallel, must have node **N1** wired in common for the circuit of Fig. 2 to operate. However, this allows an ESD event to go through a single one of the small transistors, which can result in damage to that transistor. Therefore, in addition to transistors **M3** and **M4**, another group of current path-series connected transistors whose mid-point is not wired out to any node, should be added. The width of the channels of each of these ESD protection transistors is typically 400-500 micrometers (uM). Therefore, it may not be area efficient to use the buffer **100** shown in Fig. 2 unless the current sinking requirement of the buffer makes it so large that the use of two series connected transistors is a real area savings over that required by three series connected transistors.

This is the case for many current applications, e.g., a SCSI application requiring, e.g., 48mA sink current.

Fig. 3 shows the embodiment of Figs. 1 and 2 implemented as an open drain bi-directional buffer.

In particular, as shown in Fig. 3, an input stage **150** may be added to receive the signal input at the **PAD** via transistor **M4**. The input stage **150** provides an output signal **Z** to the other portions of the integrated circuit on which the buffer is fabricated.

The buffer **100** shown in Figs. 1-3 allows 5V tolerance to be achieved in the commercial market, e.g., with an AL13 process such as is used by MAXTOR™, and with similar 3.3V processes, when the operating power supply is nominally only 2.5V or even less, e.g., 2.0V. It is area efficient for sink currents over about 30-40mA.

In the case of more moderate requirements, another embodiment of the present invention is disclosed wherein an open drain buffer capable of 16mA, is 5V tolerant in a 3.3V process technology, and is operated with only a nominal power supply of only 2.5V.

Fig. 4 shows a backgate bias generator, and Fig. 5 shows an example of a more moderate current, 5V tolerant 2.5V (or lower voltage) open drain output buffer utilizing the backgate bias generator, in accordance with another embodiment of the present invention.

In particular, Fig. 4 shows, as a part of an integrated circuit, a backgate bias generator **300** that uses two p-channel FET transistors **MB1**, **MB2** with series connected current paths between **VDD** and the **PAD**. The backgate of both transistors **MB1**, **MB2** is connected to node **BIAS** to ensure that the parasitic diodes associated with p-channel devices are always reverse biased.

The gates are cross-connected with the gate of transistor **MB1** being coupled to the **PAD**, and the gate of transistor **MB2** being coupled to **VDD**. When the **PAD** voltage is lower than **VDD**, transistor

MB1 is turned ON and **MB2** is turned OFF. Under this condition, node **BIAS** is equal to **VDD**.

When the **PAD** voltage is greater than **VDD**, **MB1** is turned OFF and **MB2** is turned ON. This connects node **BIAS** to the **PAD**.

Fig. 5 shows an exemplary 5V tolerant open drain output buffer utilizing the backgate bias generator **300** shown in Fig. 4, in accordance with another embodiment of the present invention.

In particular, the bias generator **300** of Fig. 4 is used to make the buffer **400** shown in Fig. 5 5V tolerant with a power supply **VDD** that is nominally only 2.5V (or even less, to about 2.0V).

The buffer **400** (e.g., output buffer) utilizes the same design for FET transistors **M1**, **M2**, **M3** and **M4** as shown and described with respect to Figs. 1 and 2. However, the p-channel transistor **M5** shown in Fig. 2 is not used, but instead an n-channel FET transistor **M6** is added to the top of the series current path connection of transistors **M4** and **M3**, such that there is a series current path connection of transistors **M6**, **M4** and **M3**. The other side of the current path of transistor **M6** is connected to the **PAD**, while the gate of transistor **M6** is connected to the BIAS signal generated by the backgate bias generator **300** shown in Fig. 4.

The circuit of Figs. 4 and 5 operates as follows. When signal **A** is LOW, node **N** is driven HIGH, transistors **M3**, **M4** and **M6** are turned ON, and the **PAD** is pulled LOW.

On the other hand, when signal **A** is HIGH, node **N** is driven LOW and transistor **M3** is turned OFF. At that point, if a 5V level from a legacy system connected to the buffer **400** is applied to **PAD**, the **BIAS** signal will also be at 5V. Under these conditions, node **N2** will be at a threshold voltage below the voltage level of **PAD**. For instance, the maximum voltage of node **N2**, considering an upper range of a nominal 5.0V source to be 5.5V (5.0V x 10% = 5.5V), and thus a 5.5V **PAD** signal, would be 5.5V - 0.8V = 4.7V.

At the low end of the nominal power supply voltage scale of 10% down from its nominal rating of 2.5V, or **VDD**=2.25V, then the minimum voltage at the node **N1** will be 2.25V - 0.8V = 1.45V. In this scenario, the drain-to-source voltage across transistor **M6** is 0.8V, and across transistor **M4** is 3.25V.

Fig. 6 shows the embodiment of Figs. 4 and 5 implemented as an open drain bi-directional buffer.

In particular, as shown in Fig. 6, an input stage **150** may be added to receive the signal input at the **PAD** via transistor **M4**. The input stage **150** provides an output signal **Z** to the other portions of the integrated circuit on which the buffer is fabricated.

The use of three series n-channel FET transistors **M3**, **M4**, **M6** as shown in the exemplary embodiment of Figs. 4-6 requires that each transistor be 50% larger than would be the case for a buffer with only two transistors in series. However, for ESD reasons, the minimum recommended size of the width of the channels of each of these transistors is 400-500um. The length of the channels of each of the FET transistors is typically dictated by the minimum channel length permitted by the relevant technology. The desired channel width for each of the three series transistors **M3**, **M4**, **M6** to sink 16mA is 450um, to minimize or eliminate altogether circuit area waste.

The embodiment of Figs. 4-6 of the present invention allows 5V tolerance to be achieved with 3.3V processes, when the power supply is nominally only 2.5V, or even less, e.g., only 1.8V. This embodiment is area efficient for sink currents below about 24 mA.

While the invention has been described with reference to the exemplary embodiments thereof, those skilled in the art will be able to make various modifications to the described embodiments of the invention without departing from the true spirit and scope of the invention.